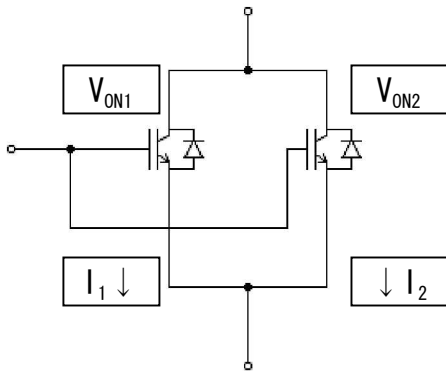


FUJI IGBT Modules U4-120 Series

2 in one-package module parallel connection application

Current imbalance in parallel connection



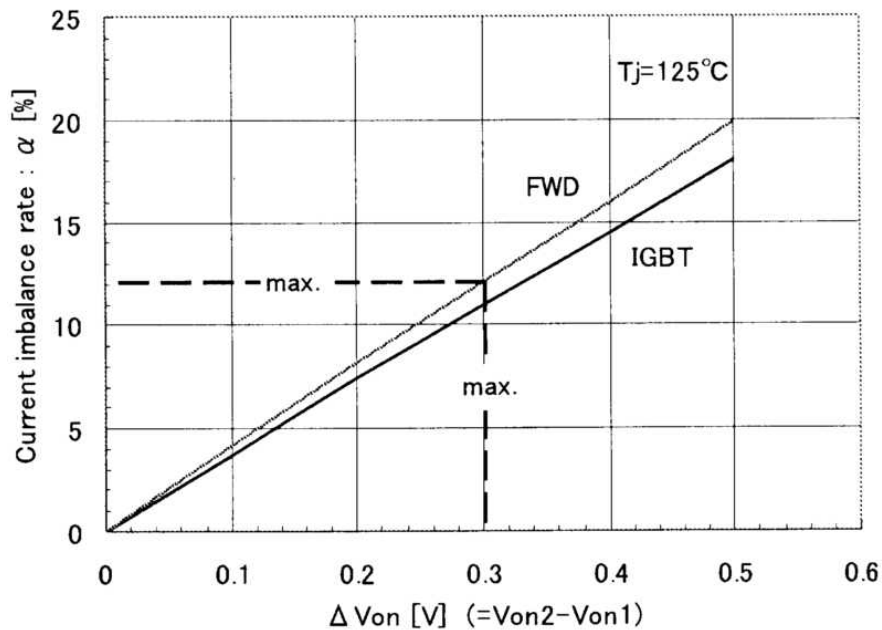
Configuration and equation

$$\Delta V_{on} = V_{on2} - V_{on1} \quad (V_{on1} < V_{on2})$$

$$I_{C(ave)} = (I_1 + I_2) / 2$$

Current imbalance was caused by difference between V_{on1} , V_{on2} , current will be divided to I_1 and I_2 respectively. In this case, the current imbalance rate is defined as following equation.

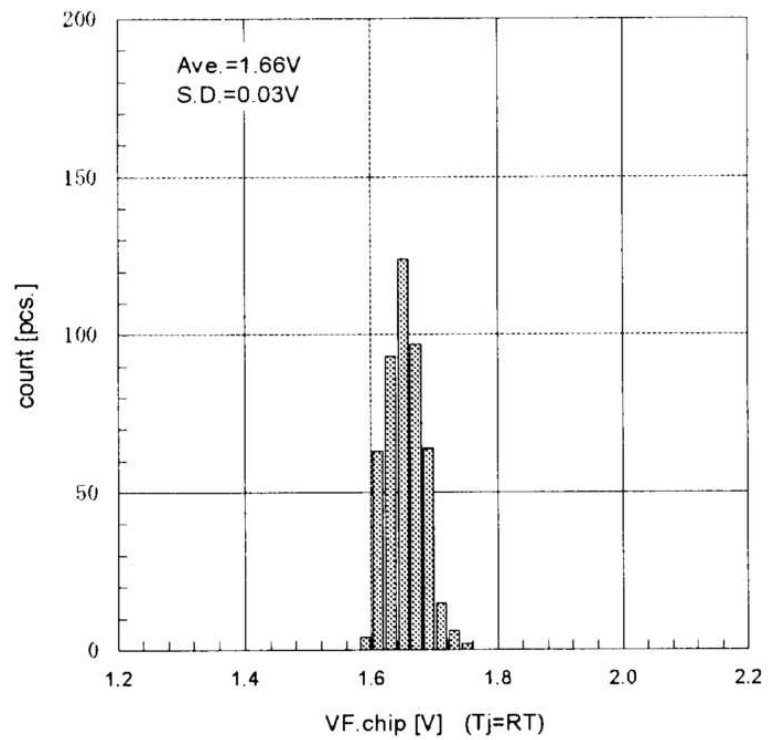
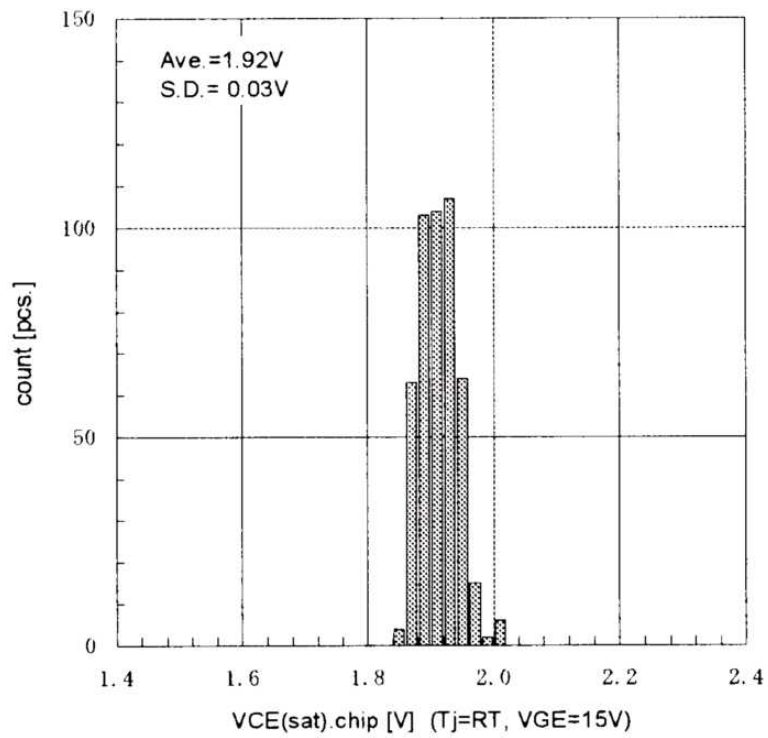
$$\alpha = [I_1 / I_{C(ave)} - 1] \times 100(\%)$$



The rank division of V_{on} is unnecessary for U4 Series by the set value of $\alpha = 12\%$ (IGBT: $\alpha = 11\%$, FWD: $\alpha = 12\%$). When connecting parallel the chips of N piece, overall permissible current is shown by the follow (I_{max} is made maximum permissible current).

$$\text{Overall permissible current } \Sigma I = I_{max} \times [1 + (n-1) \times (1 - \alpha/100) / (1 + \alpha/100)]$$

Distribution chart of $V_{CE(sat)}$ and V_F (example)



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