2nd-Generation Low Loss SJ-MOSFET with Built-In Fast Diode “Super J MOS S2FD Series”

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ABSTRACT

In order to make efficient use of energy, there has been increasing demand for enhanced efficiency in power conversion equipment, and as such, the power MOSFET mounted on this equipment are required to be compact, low loss and low noise. Fuji Electric has been developing and manufacturing products that have reduced on-state resistance and improved trade-off between turn-off switching loss and surge voltage. We have recently developed the 2nd-generation low loss SJ-MOSFET “Super J MOS S2FD Series,” which features user-friendliness and low loss, by improving its reverse recovery withstand capability through a built-in fast diode. The use of this product is expected to improve the efficiency of power conversion equipment and facilitate product miniaturization.

1. Introduction

In recent years, renewable energies such as photovoltaic power generation and wind power generation have been spreading. This has taken place against the background of global warming prevention and the Long-Term Energy Supply and Demand Outlook instituted by the Ministry of Economy, Trade and Industry of Japan. On the other hand, energy consumption has been increasing in the fields of social infrastructure, automotive, industrial machinery, IT equipment and home appliances. The importance of power conversion technology is increasing in order to use energy more efficiently. Power conversion equipment is required to provide high efficiency, high power density and low noise. In addition, the power metal-oxide-semiconductor field-effect transistor (power MOSFET) and other semiconductor switching elements used in its power conversion sections need to be compact and reduce watt loss and noise.

In order to meet such requirements, Fuji Electric has adopted a superjunction structure[(1)-(5)] since 2011. With this, it has established product lines of the 1st-generation low loss SJ-MOSFET: The “Super J MOS S1 Series” (S1 Series) that achieved both low on-state resistance and low switching loss with rated voltage of 600 V, and the “Super J MOS S1FD Series” (S1FD Series) with a built-in diode being faster than that of the S1 Series[(6)-(8)].

Moreover, we have developed “Super J MOS S2 Series” (S2 Series) based on the S1 Series by improving the trade-off relationship between the withstand voltage of the element BV_{DSS} and the on-state resistance per unit area $R_{on}{\cdot}A$. We have also achieved this by suppressing the jumping in the voltage between the drain and source (V_{DS} surge) at the time of turn-off switching[(9)].

This paper describes the 2nd-generation low loss SJ-MOSFET “Super J MOS S2FD Series” (S2FD Series) which is a product line using a built-in diode being faster than those of the S2 Series.

2. Design Concept

In order to improve the power conversion efficiency of the switching power supply, we applied the technologies of the S2 Series to the S2FD Series to make the conduction loss and turn-off switching loss E_{off} lower than those of the S1FD Series. We also worked to reduce the gate drive loss as well as the loss generated during charging/discharging of the output capacitance E_{oss} in order to suppress the circuit loss under light loads.

Current resonant and other full-bridge LLC circuits widely used for relatively large capacity power supplies in the communication and industrial sectors may cause a short circuit between the upper and lower arms during resonant breakaway. This makes the built-in diode of the MOSFET start a reverse recovery operation. The built-in diode of the MOSFET starts the reverse recovery operation at a high current change rate $-\mathrm{d}i_{DR}/\mathrm{d}t$, resulting in the generation of an excessive reverse recovery peak current. During this recovery period, the voltage change rate between the drain and source $\mathrm{d}v/\mathrm{d}t$ may rise sharply, which makes the parasitic bipolar transistor of the MOSFET operate and cause a breakdown. Consequently, products with a high reverse recovery withstand capability ($-\mathrm{d}i_{DR}/\mathrm{d}t$ withstand capability) have been used for full-bridge circuits to prevent the breakdown of MOSFET. The S2FD Series is intended to further improve the reverse recovery withstand capability of the S1FD Series that

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has been currently used for such power supplies.

3. Features

3.1 Reduced conduction loss

In order to reduce the conduction loss in the high withstand voltage power MOSFET, it is necessary to reduce the on-state resistance of the chip $R_{DS\,(on)}$ which is a dominant factor in the conduction loss. Since the size of the chip that can be mounted on the package is limited, we need to reduce the on-state resistance without increasing the chip size. For the S2FD Series, we improved the impurity diffusion process of the drift layer in the superjunction structure of the S2 Series. In this way, we maintained a high impurity concentration in the n-type region, reduced the resistance[10] and, as a result, lowered $R_{on} \cdot A$ by about 25% compared with that of the S1FD Series.

Table 1 shows the minimum $R_{DS\,(on)}$ for each package of the S2FD Series and S1FD Series with a rated voltage of 600 V. By reducing $R_{on} \cdot A$, we can mount chips with the resistance reduced from 42 mΩ to 27 mΩ, from 93 mΩ to 75 mΩ and from 132 mΩ to 84 mΩ for packages TO-247, TO-220F and TO-220 respectively. This holds promise for highly efficient power supplies.

3.2 Reduced switching loss and suppressed V_{DS} surge

When we design a circuit pattern of a power supply substrate, we often cannot create an ideal circuit pattern. This is because we reuse a pattern design of conventional power supply substrates or because of a limitation with the layout of parts. In such cases, just replacing the MOSFET to be used may cause problems of erroneous ON triggered by gate vibration during switching or an increased V_{DS} surge due to the parasitic inductance of wiring on the circuit or other causes.

To improve the flexibility of circuit pattern design of the S2FD Series, we optimized the threshold voltage to prevent erroneous ON triggered by gate vibration during switching. We also optimized the internal gate resistance to suppress the V_{DS} surge as in the case of the S2 Series.

These measures have allowed our customers to replace a conventional MOSFET with the new MOSFET without the need to change the circuit pattern or modify the component constant greatly. This means they can design highly efficient power supplies easily.

Table 1 Applicable minimum on-state resistance

Item		TO-247 package	TO-220 package	TO-220F package
Applicable minimum $R_{DS\,(on)}$	S1FD Series	42 mΩ	132 mΩ	93 mΩ
	S2FD Series (Reduction rate)	27 mΩ (36% reduction)	84 mΩ (36% reduction)	75 mΩ (19% reduction)

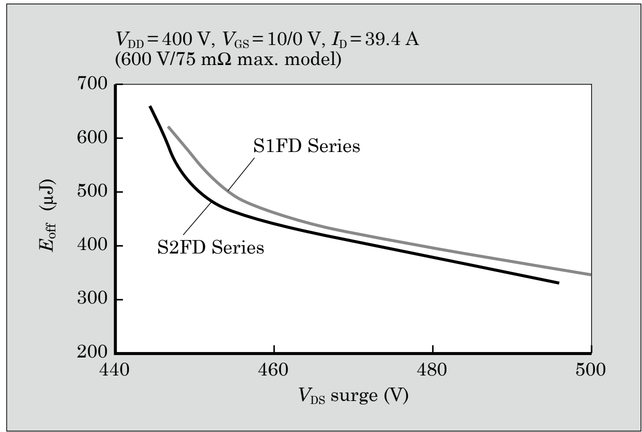

Fig.1 Trade-off characteristics between turn-off switching loss E_{off} and V_{DS} surge

We used a chopper circuit to evaluate the trade-off characteristics between E_{off} and V_{DS} surge in the S1FD and S2FD Series. Figure 1 shows the trade-off characteristics between E_{off} and V_{DS} surge. When the V_{DS} surge is the same at 480 V, the E_{off} of the S2FD Series reduced by approximately 18 μJ from that of the S1FD Series. This shows the improvement in the trade-off between E_{off} and V_{DS} surge.

3.3 Reduced watt loss under light loads

When the power supply is under light loads, the current flowing between the drain and source of the MOSFET decreases, so that the percentage of the conduction loss of the MOSFET to the watt loss of the entire power supply becomes smaller. As a result, the percentage of the gate drive loss and E_{oss} on the circuit increases. To improve the conversion efficiency of the power supply under light loads, we optimized the surface structure of the MOSFET to reduce the total gate charge Q_G and suppress the gate drive loss. We also improved the impurity diffusion process of the drift layer formed in the superjunction structure to reduce E_{oss}.

Figure 2 shows the Q_G characteristics. Compared with the S1FD Series, the S2FD Series has reduced Q_G

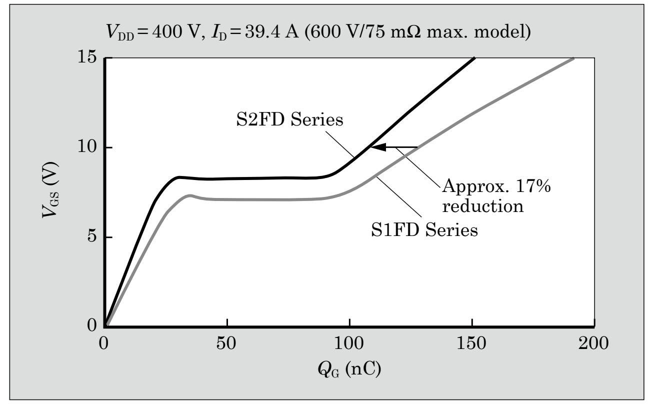

Fig.2 Total gate charge Q_G characteristics

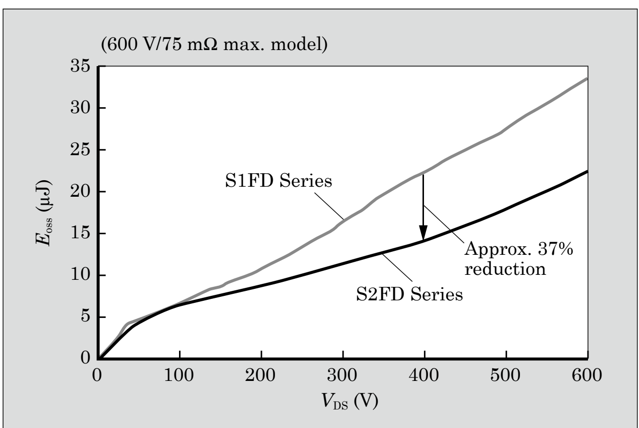

Fig.3 Loss generated during charging/discharging E_{oss} characteristics

by approximately 17% when the gate voltage V_{GS} is 10 V. Figure 3 shows the dependence of E_{oss} on the voltage between the drain and source V_{DS}. Compared with the S1FD Series, the S2FD Series has reduced E_{oss} by approximately 37% when V_{DS} is 400 V.

3.4 Improved reverse recovery withstand capability and reduced watt loss during OFF

In order to improve the reverse recovery withstand capability of the built-in diode, we used a lifetime killer to accelerate the reverse recovery operation of the built-in diode. We also reduced the reverse recovery time and reverse recovery peak current. On the other hand, the lifetime killer concentration has a trade-off relationship with the drain-source leak current I_{DSS} which is a watt loss during OFF. We therefore optimized the lifetime killer concentration and achieved better I_{DSS} characteristics while maintaining reverse recovery characteristics equivalent to the S1FD Series. As a result, we further improved the reverse recovery withstand capability.

Figure 4 shows a comparison of the reverse recovery withstand capability characteristics. The S2FD Series has achieved a 66% improvement of the reverse recovery withstand capability compared with the S1FD

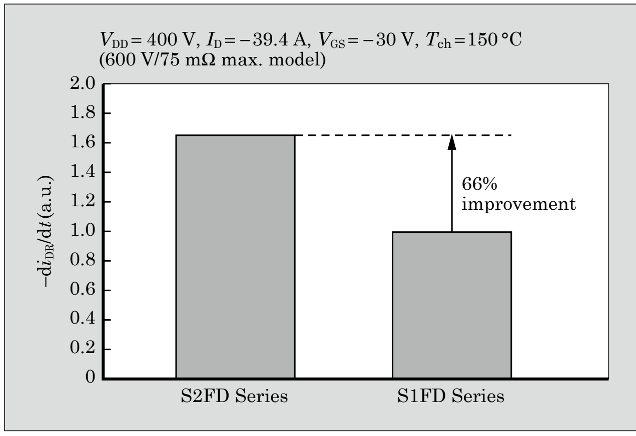

Fig.4 Reverse recovery withstand capability characteristics

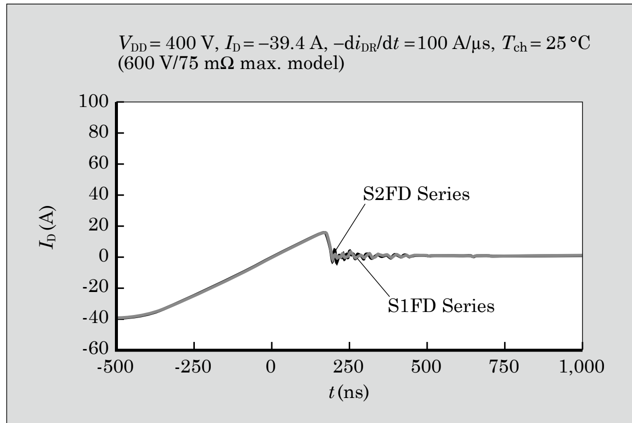

Fig.5 Reverse recovery characteristics

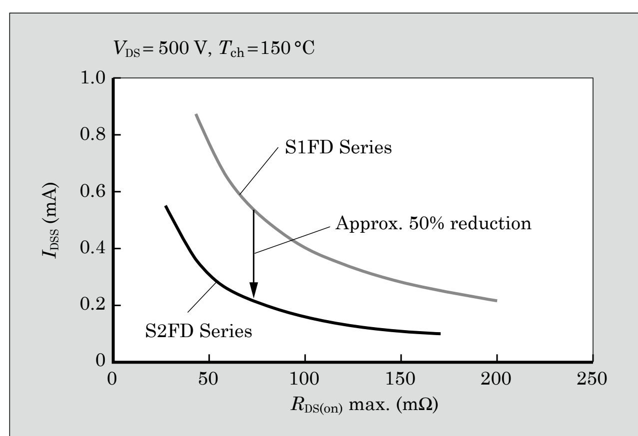

Fig.6 Drain-source leak current I_{DSS} characteristics

Series.

Figure 5 shows a comparison of the reverse recovery characteristics. The S2FD Series maintains reverse recovery characteristics equivalent to the S1FD Series.

Figure 6 shows the relationship between $R_{DS\ (on)}$ max. and the I_{DSS} characteristics. When $R_{DS\ (on)}$ max. is 75 mΩ, the S2FD Series has achieved a reduction of about 50% in I_{DSS} compared with the S1FD Series.

4. Application Effect

In order to confirm the improvements in the conversion efficiency of the power supply, we conducted a comparative evaluation of the conversion efficiency of the power supply. We did this by mounting 600 V/75 mΩ max. models of the S2FD and S1FD Series on a full-bridge LLC circuit of a power supply as shown in Fig. 7. Figure 8 shows the evaluation result. The I/O conditions for the evaluation were: Input voltage of 115 V, output voltage of 53.5 V and external gate resistance R_g of 5.1 Ω. Due to the improved characteristics and reduced losses described above, the S2FD Series achieved higher efficiency than the S1FD Series in the entire load region. In addition, the average conversion efficiency improved by 0.25 point. As a result, we

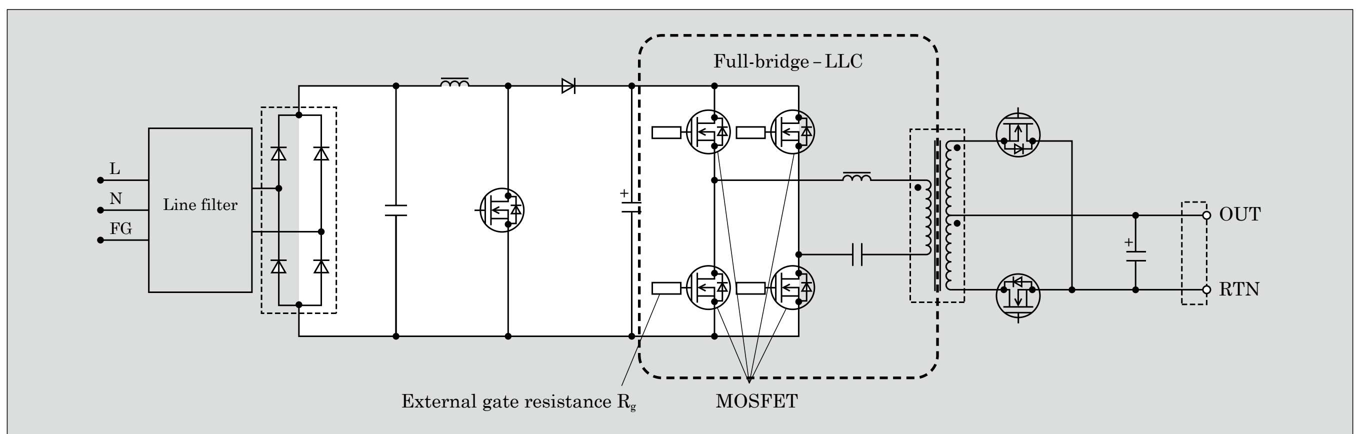

Fig.7 Full-bridge LLC circuit of power supply

Table 2 Product line-up and major characteristics of "Super J MOS S2FD Series"

V_{DS} (V)	$R_{DS(on)}$ max. (mΩ)	I_D (A)	Product line-up		
			TO-247 package	TO-220 package	TO-220F package
600	27	95.5	FMW60N027S2FD	–	–
	43	66.2	FMW60N043S2FD	–	–
	59	49.9	FMW60N059S2FD	–	–
	75	39.4	FMW60N075S2FD	–	FMV60N075S2FD
	84	37.1	FMW60N084S2FD	FMP60N084S2FD	FMV60N084S2FD
	94	32.8	FMW60N094S2FD	FMP60N094S2FD	FMV60N094S2FD
	105	29.2	FMW60N105S2FD	FMP60N105S2FD	FMV60N105S2FD
	133	22.7	FMW60N133S2FD	FMP60N133S2FD	FMV60N133S2FD
	170	17.9	FMW60N170S2FD	FMP60N170S2FD	FMV60N170S2FD

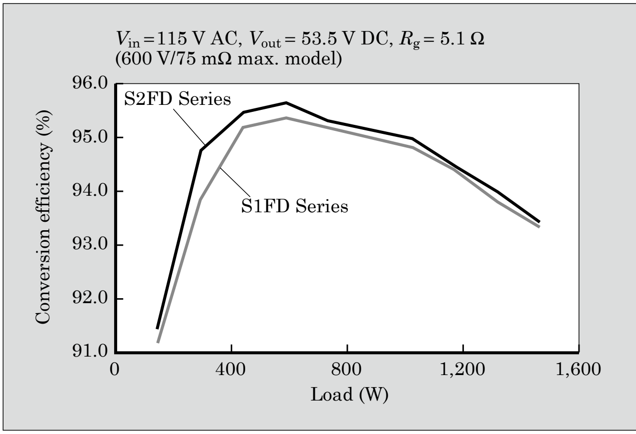

Fig.8 Conversion efficiency evaluation result

can expect a power supply design offering higher efficiency and reliability by applying the S2FD Series to a switching power supply.

5. Product Line-Up

Table 2 lists the product line-up and major characteristics of the S2FD Series.

The line-up includes products with a rated voltage V_{DS} of 600 V, on-state resistance $R_{DS(on)}$ of 27 to 170 mΩ and rated current I_D of 95.5 to 17.9 A, allowing the users to select the appropriate product for their power supply capacity.

6. Postscript

The 2nd-generation low loss SJ-MOSFET "Super J MOS S2FD Series" with a built-in fast diode is a product achieving both lower watt loss and suppressed V_{DS} surge compared with the S1FD Series. As a result, it improves the $-di_{DR}/dt$ withstand capability.

A comparative evaluation conducted by mounting the S2FD Series on a full-bridge LLC circuit has proved that it can achieve higher efficiency than the S1FD Series. This holds promise for contributing to higher efficiency and miniaturization of switching power supplies.

In order to meet further market needs, we will continue to expand the line-up of high withstand voltage models and packaged models while working to mini-

mize chip size and enhance performance such as by reducing on-state resistance.

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