1.2-kV SiC Trench MOSFET

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ABSTRACT

Fuji Electric has developed and released SiC planar gate MOSFETs. Excessive shrinkage of the cell pitch of planar MOSFETs leads to a high JFET resistance, which prevents them from achieving a low on-resistance close to the theoretical limit. To the contrary, the cell pitch of trench-gate MOSFETs can be shrunk without the increase of the JFET resistance. We have therefore developed a 1.2-kV SiC trench gate MOSFET. We have optimized the structures of the MOS channel and the JFET region, as well as reduced the cell pitch. Our trench-gate MOSFETs realize low switching loss, the increase of the threshold voltage 2.4 times, and the reduction of the on-state resistance by 48% compared with the conventional planar MOSFETs.

1. Introduction

Fuji Electric contributes to a sound material-cycle society through variety of power electronics systems utilized for railcars, automobiles, power supplies and electric power systems. Power semiconductor devices, which are core components of power electronics systems, have been evolving from those of silicon (Si) to those of silicon carbide (SiC), which is one type of wide band gap semiconductors. In the voltage rating of 1.2 kV, Si insulated gate bipolar transistors (IGBTs) have been replaced by SiC metal-oxide-semiconductor-field-effect-transistors (MOSFETs), which show lower conduction losses and switching losses than those of Si-IGBTs, due to the lower drift layer resistance of approximately one-three hundredth of that of Si[1] and no minority carriers swept during switching.

Fuji Electric has developed and released SiC planar gate MOSFETs and all-SiC modules, in which SiC planar gate MOSFETs were mounted[2],[3]. The all-SiC modules have been incorporated into our high-efficiency, compact and lightweight power conditioning sub-systems (PCSs)[4] and mega solar PCSs[5].

This paper describes our recent development of 1.2-kV SiC trench gate MOSFETs.

2. Design and Features of SiC Trench Gate MOSFETs

Compared with Si, SiC has a higher interface state density at the interface between SiO_2 as the gate oxide and SiC, and the capturing of electrons more likely to occur. As a result, there is an increase in MOS channel resistance, and this prevents SiC MOSFETs from the reduction of on-state resistance to its theoretical limit[6]. An effective means of reducing MOS channel resistance is increasing cell density (refining), as well as improving the SiO_2/SiC interface. However, excessive refinement of conventional planar gate MOSFETs results in an increase in junction field-effect transistor (JFET) resistance[1]. On the other hand, refinement of trench gate MOSFETs, which have the MOS channel oriented perpendicular to the surface, do not result in an increase in the JFET resistance, and as a result, on-state resistance can be reduced in proportion to refinement.

The cross-sectional structure of our recently developed SiC trench gate MOSFETs and a photograph of the chip are shown in Fig. 1. The development was based on the following 3 points:

(a) Improvement of the gate oxide reliability
(b) Simultaneous establishment of a high threshold voltage and a low on-state resistance
(c) Simultaneous establishment of a low on-state resistance and a high breakdown voltage

In order to improve the reliability of the gate ox-

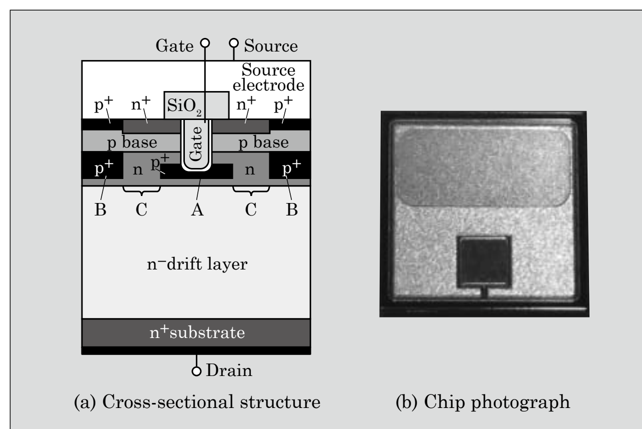

Fig.1 SiC trench gate MOSFET

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ide, it is necessary to relax the high electric field on the gate oxide at the bottom of the trench in the reverse biased mode. Therefore, we adopted a structure to cover the gate oxide at the bottom of trenches with p-wells (see A in Fig. 1). The device simulation shows that the electric field reaches a maximum at the bottom corner portion of the p-well at the bottom of the trench, and thus, we confirmed the relaxation of the electric field in the gate oxide[7].

In order to establish a high threshold voltage and low on-state resistance simultaneously, we reduced the cell pitch and optimized the MOS channel length. As shown in Fig. 2, on-state resistance decreased in proportion as the shrinkage of the cell pitch. In order to maintain a high process capability of the process, the cell pitch was set to approximately one half of that of planar gate MOSFETs.

As for the simultaneous establishment of a low on-state resistance and high breakdown voltage, we optimized the JFET regions (see C in Fig. 1), which were located in the areas between the p-wells at the bottom of the trench (see A in fig. 1) and those below the source contact (see B in Fig. 1). By making this optimization, we were able to determine multiple parameters by utilizing a device simulation[7]. The relationship between the on-state resistance and breakdown voltage trade-off is shown in Fig. 3. This optimization of the JFET region enabled us to reduce on-state resistance by about 3%, while improving breakdown voltage by about 2%.

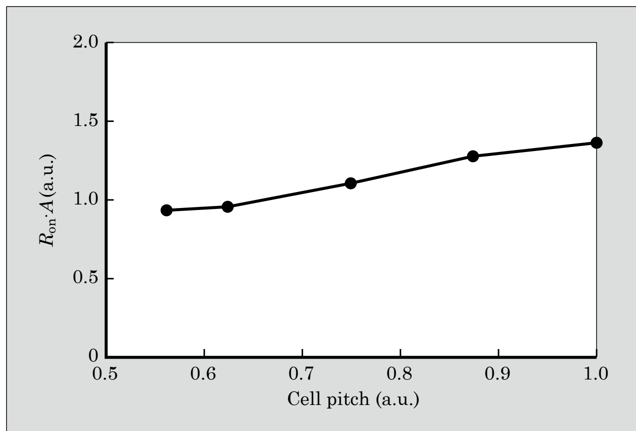

Fig.2 Cell pitch dependence of on-state resistance

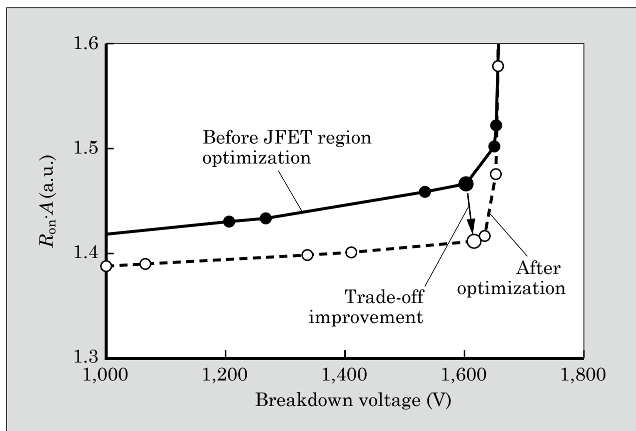

Fig.3 Relationship between on-state resistance and breakdown voltage trade-off

3. Characteristics

3.1 Static characteristics

The static characteristics of the recently developed SiC trench gate MOSFETs are shown in Fig. 4. The drain current-drain voltage characteristics in the forward biased mode at device junction temperatures of 25 °C and 175 °C are shown in Fig. 4 (a). It shows the on-state voltages at the rated current of 1.3 V at 25 °C and 2.3 V at 175 °C, respectively. The drain current-drain voltage characteristics in the reverse biased mode are shown in Fig. 4 (b). The breakdown voltages are 1.55 kV at 25 °C and 1.61 kV at 175 °C, respectively. These breakdown voltages are high enough for the devices in the voltage rating of 1.2-kV. Similar to the planar gate MOSFETs, the breakdown voltage increases in proportion as the rise in temperature.

The temperature dependencies of the threshold voltage and on-state resistance are shown in Fig. 5. The threshold voltage reduces monotonically with the temperature rise within a range from 25 °C to 200 °C, and decreases by approximately 26% at 175 °C com-

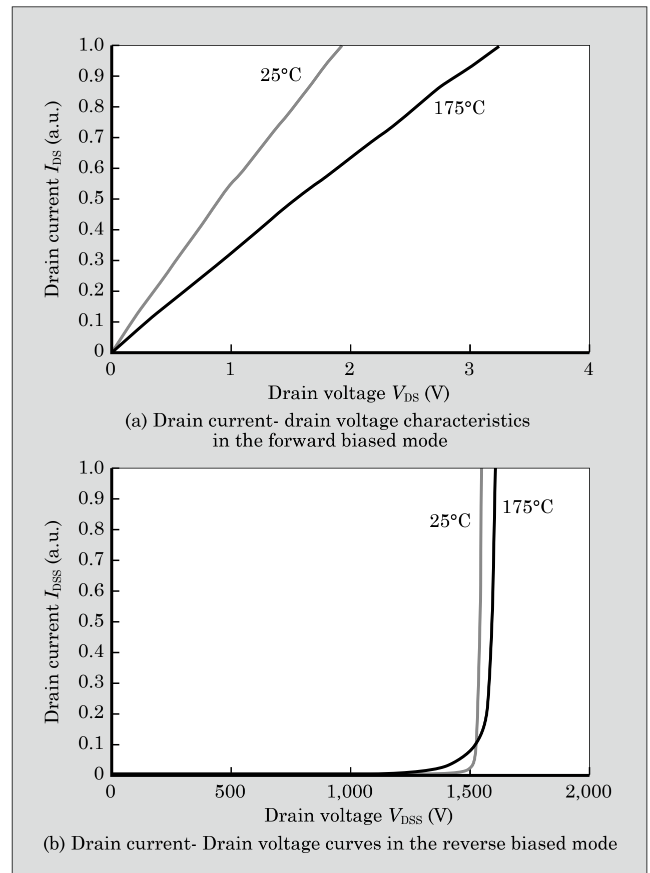

Fig.4 Static characteristics of SiC trench gate MOSFET

pared with that of 25 °C. The on-state resistance increases monotonically with the rise of temperature, and increases by approximately 57% at 175 °C compared with that of 25 °C. According to the dependence of the on-resistance on the temperature, the trench gate MOSFETs could suppress the thermal runaway in case of connecting multiple chips in parallel because temperature rise causes an increase of the on-state resistance and a decrease of the current in turn even when a current crowding occurs in a specified chip.

It should be also denoted that the trench gate MOSFETs have successfully reduced the on-state resistance normalized by unit area by approximately 50% compared with the planar gate MOSFETs. The trench gate MOSFETs are expected to contribute to further reduction of the cost in overall systems in terms of the miniaturization of cooling components and the improvement of efficiency in modules and power electronics systems.

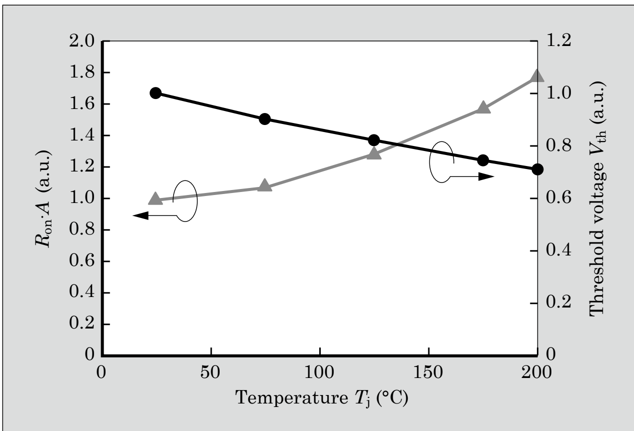

Fig.5 Temperature dependencies of threshold voltage and on-state resistance

3.2 Switching characteristics

The switching test circuit and the typical turn-on and turn-off waveforms are shown in Fig. 6. The turn-on time, which is defined by the duration from the time of V_{GS}=0 V until the time that drain current reaches 90% in the on state, is approximately 60 ns. The turn-off time, which is defined by the duration from the time that the gate voltage is 90% in the on state until the time the drain current reaches 10% in the on state, is approximately 75 ns.

The gate resistance dependence of the switching

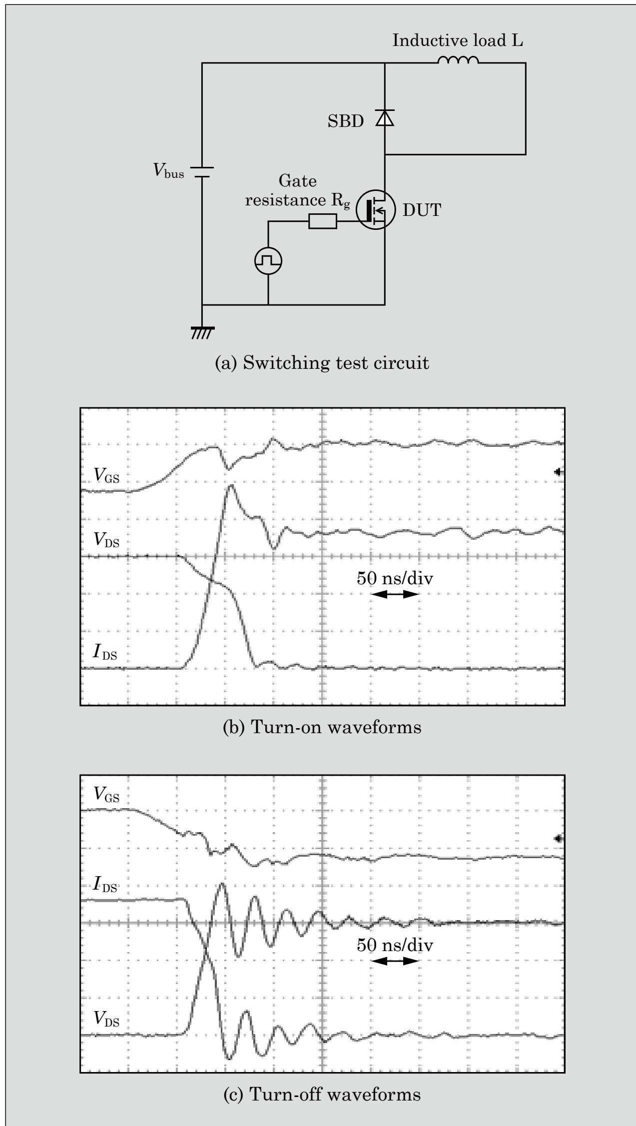

Fig.6 Switching test circuit and typical waveforms

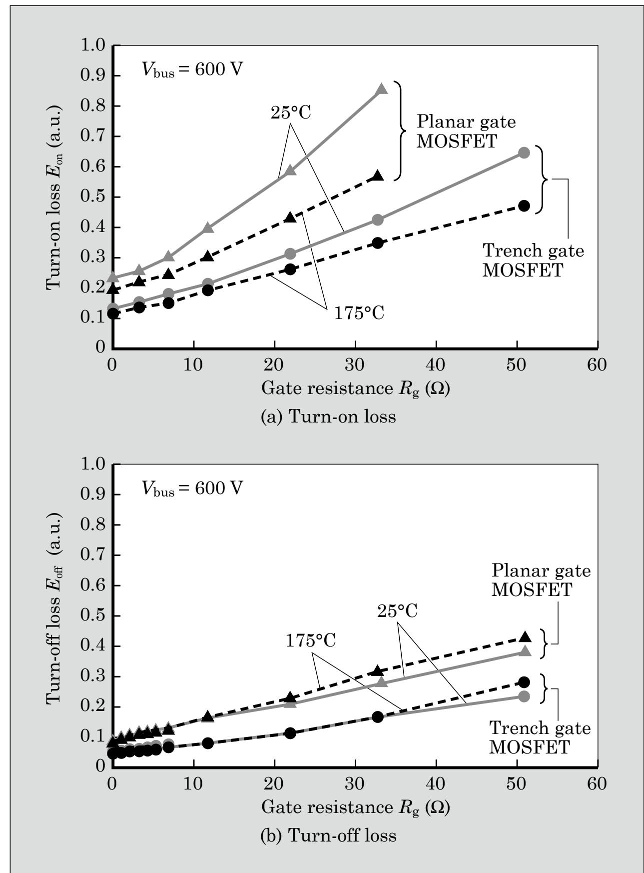

Fig.7 Gate resistance dependence of switching loss

loss is shown in Fig. 7. Under the condition of drain voltage of 600 V, gate resistance of 22 Ω and the temperature of 25 °C, the trench gate MOSFET could reduce turn-on loss by 47% and turn-off loss by 48% compared to the planar gate MOSFETs. The reason for this is most likely due to the fact that feedback capacitance C_{rss} is smaller for the recently developed trench gate MOSFETs than for the planar gate MOSFETs.

The turn-on loss is lower at 175 °C than at 25 °C. The reason for this is thought to be the short charging time for the gate due to the lower threshold voltage at 175 °C than that at 25 °C. On the other hand, the turn-off loss at 175 °C is slightly higher. This is thought to be due to the longer discharge time for the gate because the difference between the drive gate voltage and threshold voltage is somewhat larger at 175 °C than that at 25 °C.

3.3 Short-circuit and avalanche withstanding capabilities

The waveforms before rupture under the short-circuit capability test at a drain voltage of 800 V and at the temperature of 175 °C are shown in Fig. 8. We confirmed a sufficiently high enough short-circuit capability of 9.8 µs.

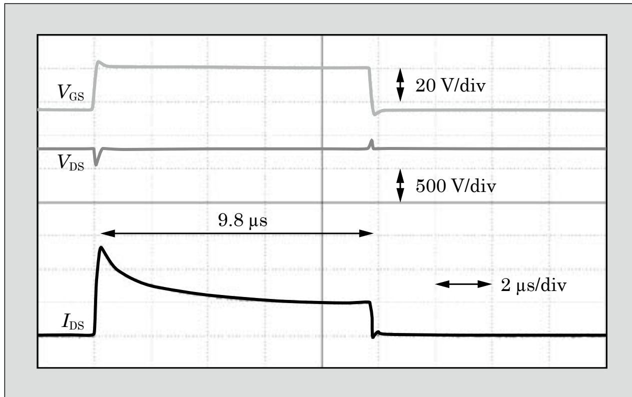

Fig.8 Waveforms during short-circuit capability test

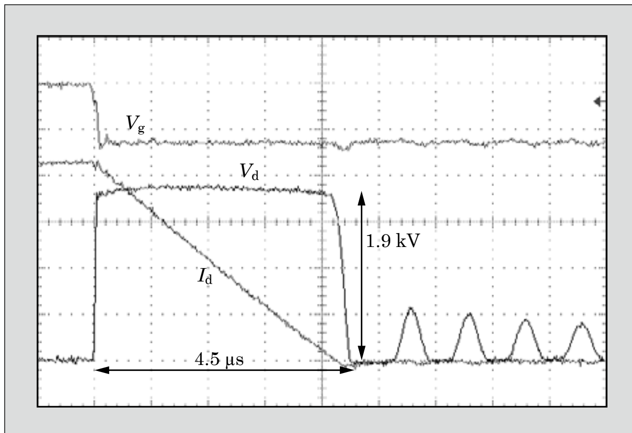

Fig.9 Waveforms during avalanche withstanding capability test

The waveforms during the avalanche withstanding capability test at an inductive load of 100 µH and at the temperature of 175 °C are shown in Fig. 9. The avalanche withstanding energy was 6.0 J/cm^2, and this was at the same level as the planar gate MOSFETs.

4. Postscript

This paper described the recent development of 1.2-kV SiC trench gate MOSFETs in Fuji Electric.

By the shrink of the cell pitch and the optimization of the channel length, our recently developed SiC trench gate MOSFETs have achieved higher threshold voltages and lower on-state resistances than SiC planar gate MOSFETs. In the future, we will endeavor for the further improvement of the quality at the SiO_2/SiC interface in order to decrease on-state resistance.

Some of our research was carried out as part of a project of the joint research body "Tsukuba Power Electronics Constellations (TPEC)." We would like to conclude by expressing our appreciation to all those involved in the project.

References

(1) B.J.Baliga, POWER SEMICONDUCTOR DEVICE, PWS Publishing Company.

(2) Nakano, H. et al. Ultra-Compact, High-Reliability All-SiC Module. FUJI ELECTRIC REVIEW. 2013, vol.59, no.4, p.221-225.

(3) Nakamura, H. et al. All-SiC Module Packaging Technology. FUJI ELECTRIC REVIEW. 2015, vol.61, no.4, p.224-227.

(4) Matsumoto, Y. et al. Power Electronics Equipment Applying SiC Devices. FUJI ELECTRIC REVIEW. 2015, vol.58, no.4, p.212-216.

(5) Oshima, M. et al. Mega Solar PCS Incorporating All-SiC Module "PVI1000 AJ-3/1000". FUJI ELECTRIC REVIEW. 2015, vol.61, no.1, p.11-16.

(6) T.Kimoto and J.A.Cooper, FUNDAMENTALS OF SILICON CARBIDE TECHNOLOGY, 2014 John Wiley & Sons.

(7) Kobayashi, Y. et al. Simulation Based Prediction of SiC Trench MOSFET Characteristics. FUJI ELECTRIC REVIEW. 2016, vol.62, no.1, p.12-16.

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