HVIC Technologies for IPM

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ABSTRACT

A high voltage integrated circuit (HVIC), which is a gate driver IC with a high breakdown voltage, is one of the key devices required in enhancing the functionality of intelligent power modules (IPMs). Fuji Electric has developed HVIC technology characterized by its advanced functionality, compactness, high reliability, and guaranteed industrial use at 600 V/1,200 V for small- and medium-capacity IPM. By reducing the circuit area and adopting high breakdown voltage technology and enhanced noise resistant level-shift circuit technology, we have reduced the chip size by 20% while improving the breakdown voltage and reliability. In addition, we have achieved over-current and overheat protection circuit technology for upper-arm IGBT, as well as level-down functionality for alarm signals.

1. Introduction

An intelligent power module (IPM) is a power semiconductor module that integrates into one package a driver IC with the gate drive and protective functions together with insulated-gate bipolar transistors (IGBTs) or other power switching devices and free wheeling diodes (FWDs). IPMs help reduce the number of parts and size and simplify the design of systems and are used in wide-ranging applications including industrial machines, consumer electronics such as air conditioners and power supply equipment for servers.

Fuji Electric developed the world's first IPM using bipolar transistors in 1986. Ever since then, we have been actively developing products that help to improve the reliability and reduce the size of systems. One such product was the world's first IPM equipped with an IGBT chip overheat protection function that we released in 1997[1]. In 2012, we commercialized a small-capacity IPM for inverter air conditioners. It eliminates the need for an external insulation circuit or level-shift circuit by employing a high-voltage integrated circuit (HVIC), which is a high breakdown voltage gate driver IC. Furthermore, we are working on ways to incorporate HVICs in medium-capacity IPMs for industrial use.

HVICs to be mounted on IPMs are required to withstand 600 V and 1,200 V according to the breakdown voltage class of the IPM. In addition, they must also offer high reliability to withstand the noise caused by IGBT switching, integrate various protection circuits and have a small chip size.

Based on the 800-V breakdown voltage guaranteed HVIC technology[2] developed in 2010, Fuji Electric has developed new industrial 600-V/1,200-V breakdown voltage guaranteed HVIC technology. It features high functionality, compactness and high reliability and is intended for small- and medium-capacity IPMs of up to the 1,200-V/100-A class. Of the new technology, this paper describes the device-process technology and circuit component technology.

2. Features of HVIC for IPMs

Figure 1 shows the 1,200-V breakdown voltage guaranteed HVIC chip prototyped for medium-capacity IPMs and Fig. 2 a block diagram of its circuit and peripheral circuit. One feature of the HVIC is that it integrates 3 circuits into one chip: a low-side circuit operated based on the ground potential, high-side circuit operated based on the source potential of the upper-arm IGBT to provide the gate drive function, and level-shift circuit responsible for the level-up function for control signals. The source potential of the upper-arm IGBT may vary from about −100 to over +1,000 V along with switching and a high isolation breakdown voltage is provided between the high-side and low-side

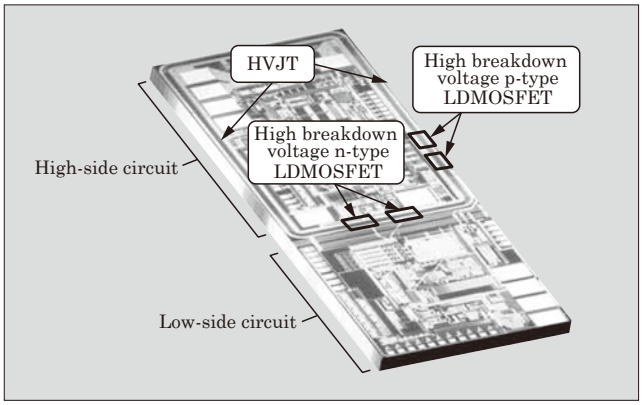

Fig.1 1,200-V breakdown voltage guaranteed HVIC chip

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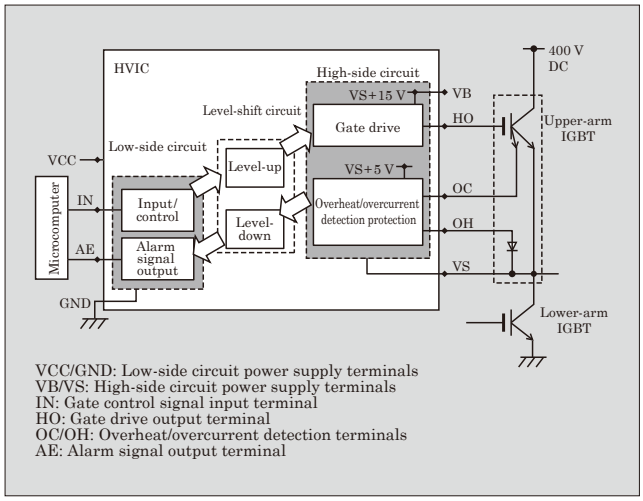

Fig.2 Block diagram of 1,200-V breakdown voltage guaranteed HVIC circuit and peripheral circuit

circuits.

With the HVIC, the control signal based on the ground potential input to the low-side circuit is transmitted through the level-shift circuit to the gate drive circuit in the high-side circuit, which drives the upper-arm IGBT. With an IPM incorporating the HVIC, this level-shift function makes it possible to drive the upper-arm IGBT without using an optocoupler or other insulation device.

Features of the 1,200-V breakdown voltage guaranteed HVIC include:

(a) Guaranteed breakdown voltage of 1,200 V, power supply voltage of up to 24 V (guaranteed breakdown voltage 800 V with the previous product)

(b) Provision of overheat/overcurrent detection protective function for upper-arm IGBT

(c) Provision of level-down function for alarm signals

(d) Reduction of circuit area and adoption of high breakdown voltage technology (in-chip wire bonding high potential wiring technology with the previous product)

(e) Enhanced noise immunity (dV/dt noise immunity ±50 kV/μs min.)

3. Device-Process Technology

To achieve a compact and high-reliability HVIC with advanced-functionality, we have developed 600-V/1,200-V high breakdown voltage CMOS process that introduces a new well structure and high breakdown voltage technology. For device isolation, the self-isolation method has been employed.

3.1 Reduction of circuit area by using divided high-side well structure

Figure 3 shows the cross-sectional structure of the HVIC. The HVIC is provided with a low-side well for forming the low-side circuit and high-side well for forming the high-side circuit. Both are composed of an n-type diffusion layer on the p-type substrate. The high-side well is separated from the low-side well by the high-voltage junction termination (HVJT) and the HVJT functions to maintain the high breakdown voltage between the high-side and low-side circuits.

(1) Issue with conventional high-side well structure

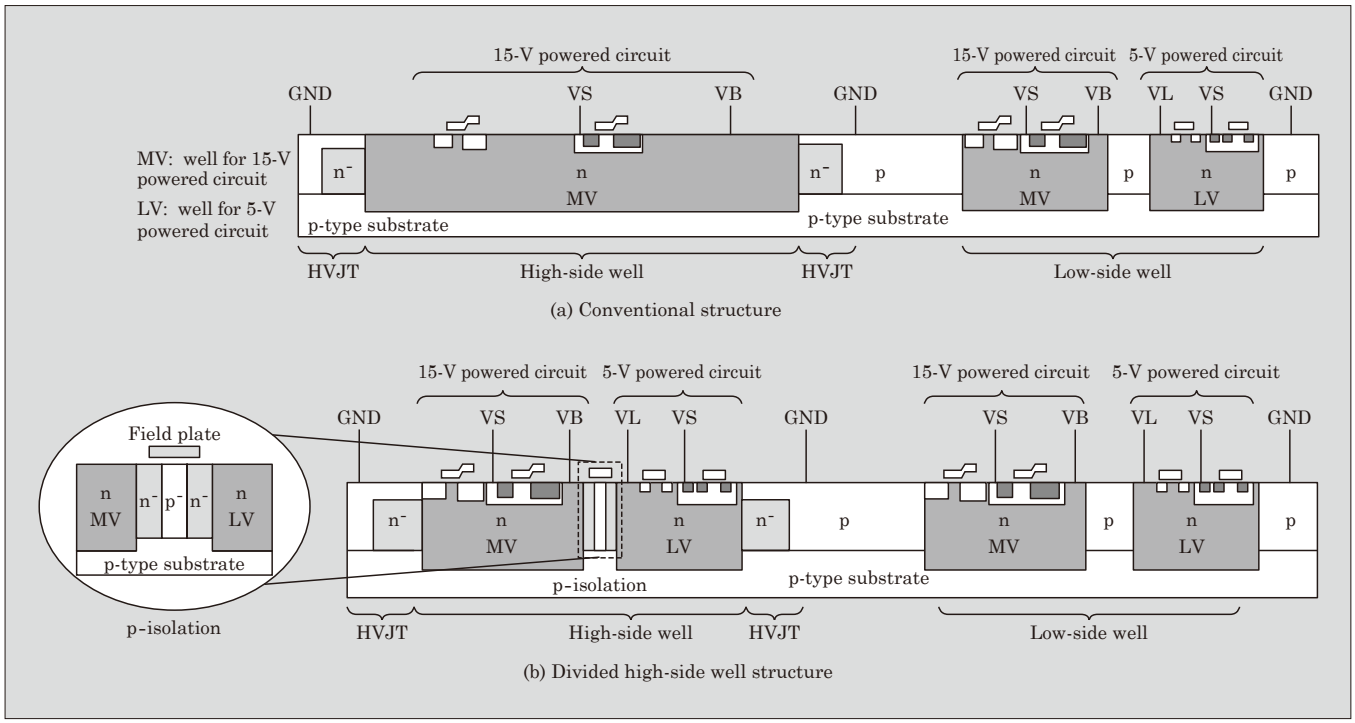

Fig.3 Cross-sectional structure of HVIC

As shown in Fig. 3(a), the low-side well is composed of multiple diffusion layers corresponding to the power supply voltages of the individual circuits. However, the high-side well is composed of a single diffusion layer in the conventional HVIC. This is because it was difficult to divide the high-side well while maintaining the high breakdown voltage with the conventional technology. For that reason, the high-side circuit could only support one power supply voltage, which reduced the degree of freedom of circuit design.

(2) Divided high-side well structure

For the purpose of solving the issue described above, we have developed the divided high-side well structure. Figure 3(b) shows the cross-sectional structure of the HVIC that uses the divided high-side well structure. The high-side well is composed of 2 diffusion layers corresponding to 2 power supply voltages. A structure called p-isolation, which consists of low-concentration n-type and p-type diffusion layers, is used to separate the 2 diffusion layers from each other while the high breakdown voltage of the high-side well is maintained. This allows multiple power supply voltage circuits to be used for configuring a circuit for the high-side circuit in the same way as the low-side circuit. This improvement of the degree of design freedom has made it possible to realize a high-side circuit such as the protective circuit with an area reduced by approximately 20% from the previous product.

3.2 High breakdown voltage technology using area-saving self-shielding method

The level-shift circuit has the role of transmitting signals from the low-side circuit to the high-side circuit. And, when the high-side circuit is activated based on 400 V, for example, the level-shift circuit must convert signals based on the ground potential to those based on 400 V. This level-up function is realized by using high breakdown voltage n-type laterally diffused metal-oxide-semiconductor field-effect transistors (LDMOSFETs). Figure 4 shows the n-type LDMOSFETs of the 600-V breakdown voltage guaranteed HVIC chip.

(1) Conventional high breakdown voltage n-type LDMOSFET

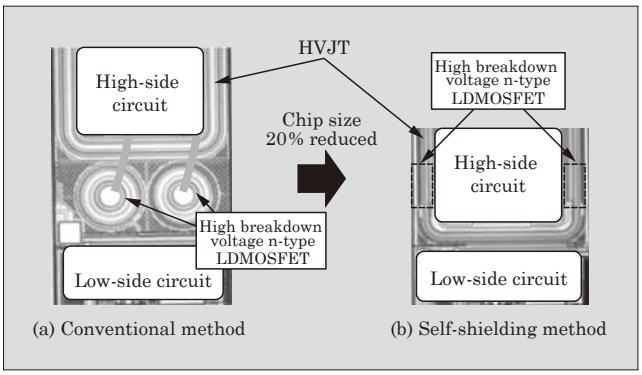

Fig.4 n-type LDMOSFETs of 600-V breakdown voltage guaranteed HVIC chip

Figure 4(a) shows the 600 V guaranteed HVIC chip with conventional high breakdown voltage n-type LDMOSFETs that use wire bonding. With the conventional HVIC, the high breakdown voltage n-type LDMOSFETs occupied a large portion of the area in the chip.

(2) High breakdown voltage n-type LDMOSFET of self-shielding type

In order to reduce the chip size, we have employed the self-shielding method that makes a high breakdown voltage possible with a reduced area. We have developed 600-V and 1,200-V guaranteed HVICs incorporating high breakdown voltage n-type LDMOSFETs. Figure 4(b) shows the 600-V guaranteed HVIC chip with the high breakdown voltage n-type LDMOSFETs using the self-shielding method. The self-shielding method integrates the high breakdown voltage n-type LDMOSFET and HVJT. It allows the device footprint to be reduced from the conventional method that requires independent high breakdown voltage n-type LDMOSFETs. This technology has meant we could successfully reduce the chip size by 20% from the previous product[3].

3.3 Level-down high breakdown voltage device technology

(1) Level-down function

The prototyped 1,200-V breakdown voltage guaranteed HVIC is equipped with the level-down function for alarm signals. This allows alarm signals for notification of errors of the upper-arm IGBT chip, such as overheat and overcurrent, to be transmitted to the external microcomputer without requiring any external insulation device or level-shift circuit.

An alarm signal output from the abnormal detection circuit in the high-side circuit is converted into a signal based on the ground potential by the level-down function of the level-shift circuit to be transmitted to the microcomputer through the low-side circuit. While the level-up function of the level-shift circuit is realized by using the high breakdown voltage n-type LDMOSFET, the level-down function uses the high breakdown voltage p-type LDMOSFET.

(2) Device structure

Figure 5 shows the device structure of the 1,200-V breakdown voltage guaranteed p-type LDMOSFET that has been developed. As with the high breakdown voltage n-type LDMOSFET, the structure integrates the HVJT by using the self-shielding method. In order to guarantee the 1,200-V breakdown voltage, a high breakdown voltage structure called the double RESURF structure and resistive field plate (RFP) structure have been employed. The double RESURF structure consists of a 3-layer structure including the p-type substrate, n-type diffusion layer and p-type diffusion layer on the surface. The n-type diffusion layer and the p-type diffusion layer of the surface become

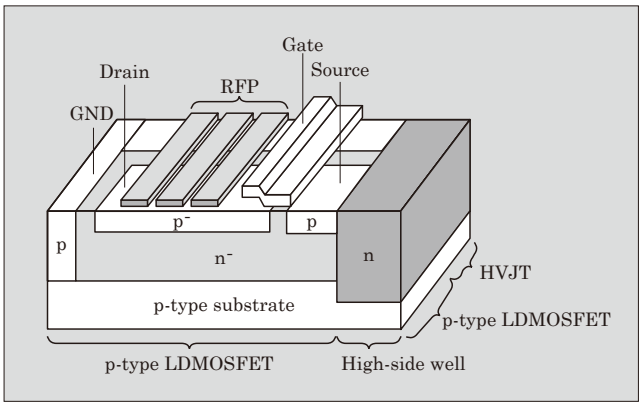

Fig.5 Device structure of 1,200-V breakdown voltage guaranteed p-type LDMOSFET

completely depleted when a high voltage is applied, which mitigates the electric field. The RFP structure has a polysilicon resistor with the electrodes at both ends connected to the high potential and ground potential provided in the high breakdown voltage region. The uniform potential gradient generated in the polysilicon resistor mitigates the electric field in the high breakdown voltage region. These structures are also used for the HVJT and high breakdown voltage n-type

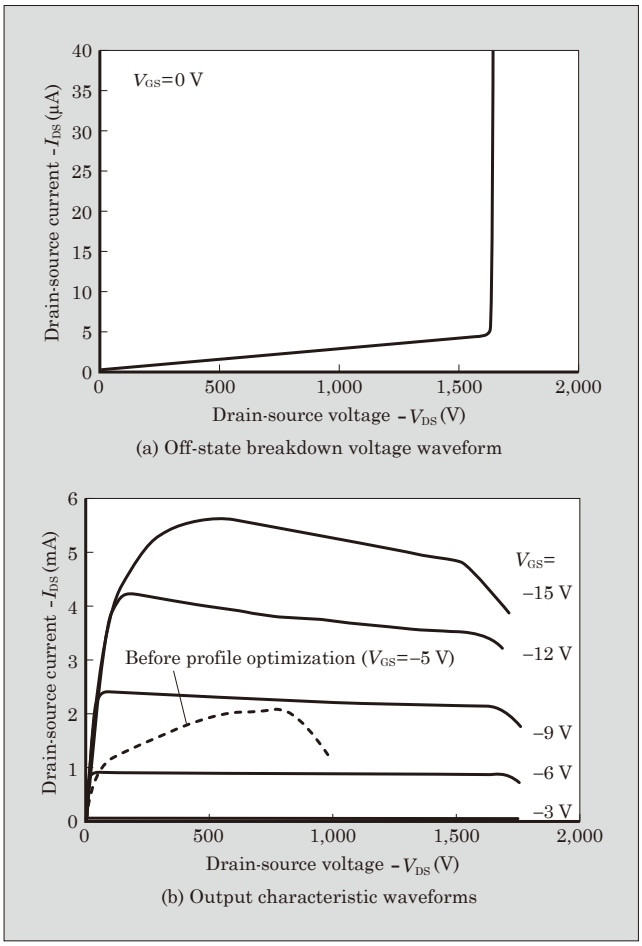

Fig.6 Characteristics of 1,200-V breakdown voltage guaranteed p-type LDMOSFET

LDMOSFET.

(3) Characteristics

Figure 6 shows the characteristics of the 1,200-V breakdown voltage guaranteed p-type LDMOSFET. Figure 6(a) shows an off-state breakdown voltage waveform. Although being a lateral device, it realizes an actual breakdown voltage of approximately 1,640 V. The leakage current observed in the region under 1,700 V is due to the current flowing in the RFP structure. By optimizing the resistance value of the RFP structure, a low leakage current of 5 μA or less at room temperature is achieved while the high breakdown voltage is maintained.

Figure 6(b) shows output characteristic waveforms. At the gate-source voltage of −15 V and drain-source voltage of −400 V, a drain current of 5.4 mA is obtained and the on-state breakdown voltage of approximately 1,500 V is realized. The dotted line in Fig. 6(b) shows the characteristic of the device prototyped in the initial stage of development. The current decrease observed around −800 V is due to the substrate leakage phenomenon recently discovered, which has limited the on-state breakdown voltage to −800 V. Fuji Electric has clarified the detailed mechanism of how this phenomenon is generated and used the results as the basis for optimizing the diffusion layer profile. This has led to a reduction in the substrate leakage phenomena to −1,500 V, which has resulted in the realization of a high on-state breakdown voltage.

4. Circuit Component Technology

4.1 High noise immunity level-shift circuit technology

(1) Conventional level-shift circuit

Figure 7 shows the conventional level-shift circuit for level-up shifting. It is composed of 2 sets of common-source amplifier circuits each using a level-shift resistor and a high breakdown voltage n-type LDMOSFET and the latch circuit in the high-side circuit.

By inputting a control signal from the low-side circuit to the common-source amplifier circuits, a voltage drop according to the control signal is generated in

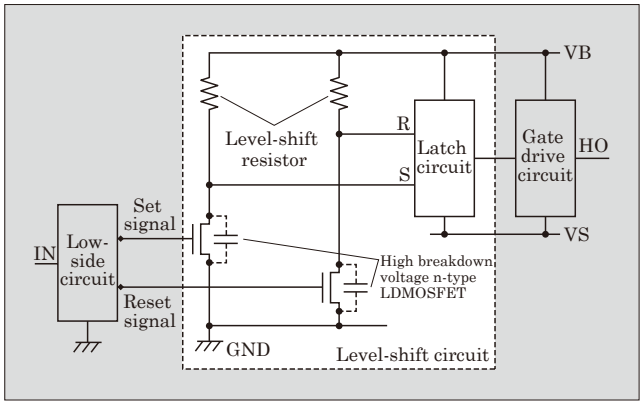

Fig.7 Conventional level-shift circuit for level-up shifting

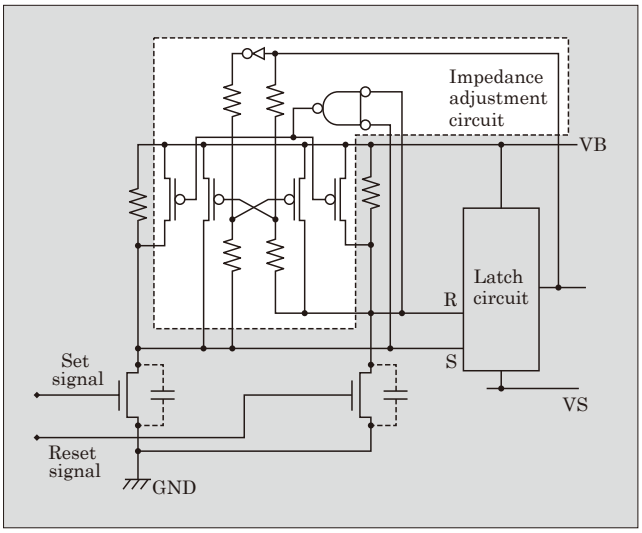

Fig.8 Impedance conversion type level-shift circuit

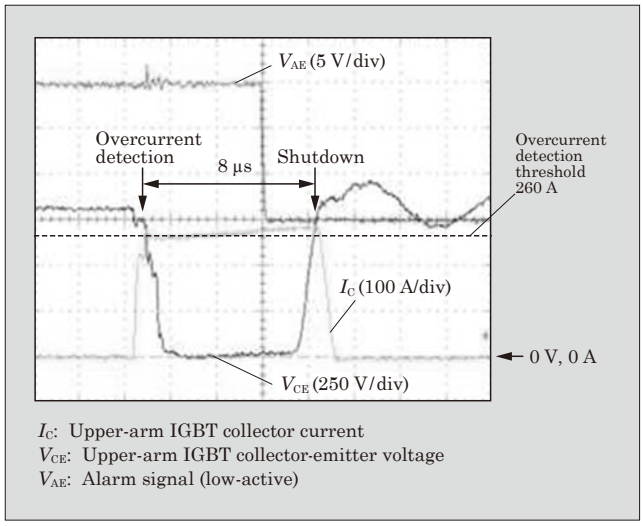

Fig.9 Overcurrent test waveforms of 1,200-V/100-A class IPM incorporating HVIC

the level-shift resistors, which switches the output of the latch circuit. This operation transmits the signals from the low-side circuit to the high-side circuit.

(2) Circuit malfunction caused by dV/dt noise of conventional circuit

The conventional level-shift circuit had an issue of being susceptible to malfunctions due to dV/dt noise. The dV/dt noise is generated by rapid variations in the reference potential of the high-side circuit due to switching of the upper-arm IGBT. This dV/dt noise causes a noise current to flow in the level-shift resistors, which generates a voltage drop. And the output of the latch circuit and the output of the subsequent gate drive circuit might be inverted erroneously.

(3) Impedance conversion type level-shift circuit

Figure 8 shows the impedance conversion type level-shift circuit[4] newly developed for improving the dV/dt noise immunity. The MOSFETs for impedance adjustment are connected in parallel with the level-shift resistors. This structure dynamically optimizes the impedance of the level-shift resistors according to the output status of the latch circuit. In this way, the voltage drop in the level-shift resistors due to the dV/dt noise current is controlled to prevent a malfunction.

4.2 Overheat/overcurrent protection circuit technology

The HVIC developed is equipped with an overheat/overcurrent protection circuit in the high-side well for protecting the upper-arm IGBT from overheating and overcurrent.

Overcurrent detection is achieved by monitoring the current flowing in the current sensing IGBT integrated in the IGBT chip. This is done by using the shunt resistor integrated in the HVIC. Overheat detection is achieved by monitoring the junction voltage of the temperature sensing diode.

Figure 9 shows overcurrent test waveforms of the 1,200-V/100-A class IPM that incorporates the HVIC prototyped. Immediately after an overcurrent exceeding 260 A flows in the upper-arm IGBT, an alarm signal indicating an overcurrent is output and the gate output of the HVIC is shut down. The time from the generation of the overcurrent to the shutdown is around 8 μs, which indicates that high-speed response sufficient for protecting the IGBT is possible.

5. Postscript

This paper has described the new HVIC technology for IPMs that has been developed. This technology realizes enhanced functionality and improved reliability of IPMs and helps to improve the reliability and reduce the size of power conversion systems. We intend to continue developing power IC technologies that help enhance the value of power conversion systems.

References

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